**In the Claims:**

1. (Currently Amended) An electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages, each pipeline stage generating pipeline data; ~~and~~

a latch positioned between the pipeline stages; and

wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode ~~comprising~~ including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the ~~instruction~~ generated pipeline data to propagate, independent of the enable signal, through ~~the first and second pipeline stages without being stored in the latch; in which the latch is held open so that the instruction propagates through the first and second pipeline stages without being stored in the latch~~ the latch; and

wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

2. (Original) An electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode, and to hold the latch open when the electronic circuit is in the reduced mode.

3. (Previously presented) An electronic circuit as claimed in claim 2, wherein the latch control circuit receives the control signal indicating the mode of operation of the electronic circuit.

4. (Original) An electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage.

5. (Original) An electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the third type is processed.

6. (Original) An electronic circuit as claimed in claim 5, wherein, after the instruction of the third type is processed, the electronic circuit is adapted to operate in the reduced mode if the following instruction is of the second or third type.

7. (Original) An electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type is processed.

8. (Original) An electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction.

9. (Original) An electronic circuit as claimed in claim 1, wherein the second type of instruction includes an arithmetic computation instruction.

10. (Original) An electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions.

11. (Original) An electronic circuit as claimed in claim 1, wherein the first pipeline stage comprises a data memory.

12. (Original) An electronic circuit as claimed in any claim 1, wherein the second pipeline stage comprises a write back stage.

13. (Currently Amended) A method of operating an electronic circuit, the electronic circuit being adapted to process a plurality of types of instruction, the electronic circuit comprising first and second pipeline stages and a latch positioned between the stages, the method comprising:

~~operating~~ controlling modes of the electronic circuit ~~controlled by~~ in response to a control signal that is based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode ~~comprising~~ including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the instruction to propagate, independent of the enable signal, through ~~the first and second pipeline stages without being stored in~~ the latch; wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

14. (Currently amended) A method as claimed in claim 13, wherein the step of controlling the electronic circuit [[is]] further includes ~~adapted to~~ processing a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage.

15. (Original) A method as claimed in claim 14, further comprising the step of operating the electronic circuit in the normal mode until an instruction of the third type is processed.

16. (Original) A method as claimed in claim 15, wherein, after processing the instruction of the third type, the method further comprises the step of operating the electronic circuit in the reduced mode if the following instruction is of the second or third type.

17. (Original) A method as claimed in claim 14, further comprising the step of operating the electronic circuit in the reduced mode until an instruction of the first type is processed.

18. (Original) A method as claimed in claim 13, wherein the first type of instruction includes a load instruction.

19. (Original) A method as claimed in claim 13, wherein the second type of instruction includes an arithmetic computation instruction.

20. (Original) A method as claimed in claim 14, wherein the third type of instruction includes compare, store, branch and jump instructions.